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(54) Computer testing capture device

(57) A capture device for use in testing a target computer 7 has a screen capture circuit 2 including a decode circuit 18 which reads pixel control signals transmitted to a target screen 17, to generate bytes for storage in a capture memory 19 and control signals for a memory pointer circuit 20. This allows monitoring of what is actually displayed on a target screen 17 rather than what is transmitted to the target screen memory 15. The device also includes a serial capture circuit (3, Fig 1) which carries out monitoring and/or simulation of transmitted or received serial signals for the target computer 7.

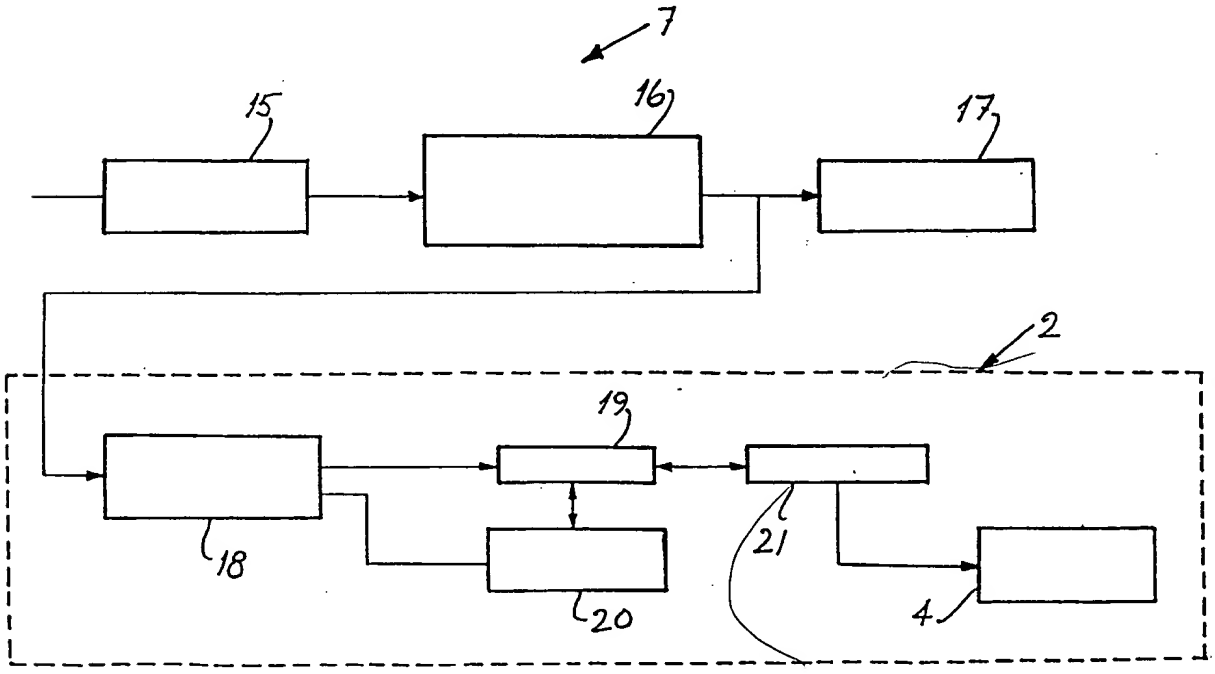

Fig.2

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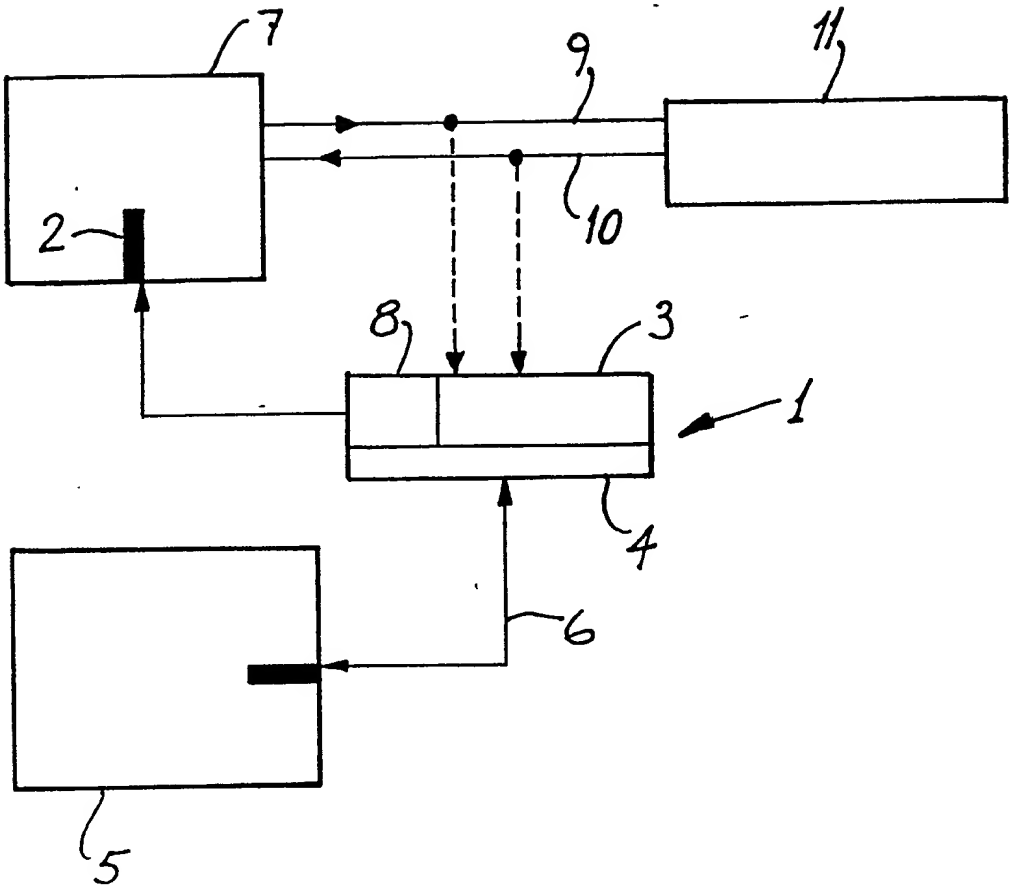

Fig. 1

"A computer testing capture device"

The invention relates to a capture device for use in testing of a target computer.

Heretofore, capture devices have included screen capture circuits which are constructed to read data transmitted to a screen memory of a target computer. The screen data is read from the screen memory and transmitted to a host computer where the data is stored either for recording as a reference target computer output or for comparison with a reference. However, the screen data is generally a representation of what is displayed on the screen, for example, the letter "A" as seen on the screen is actually stored in screen memory as 41 Hex in some target computers. In such a situation, the screen capture circuit would only know that a representation of the letter "A" has been transmitted to the screen memory and it does not known what is actually displayed on the target screen. Accordingly, character fonts used and the manner (e.g. colour) in which pixels are displayed are not checked.

The invention is directed toward providing a capture device to overcome these problems.

According to the invention, there is provided a computer testing capture device comprising a screen capture circuit comprising:-

a decode circuit for decoding pixel control signals of a target screen and generating decoded data bytes representing displayed pixels;

a capture memory for the decoded data bytes;

an output interface for reading the decoded data for transmission to a host computer; and a capture memory address pointer circuit for directing access of the output interface to the capture memory, and wherein the decode circuit comprises means for controlling the pointer circuit in response to position control signals within the pixel control signals.

In one embodiment, the device further comprises a serial capture circuit comprising means for monitoring and simulation of serial data flow between a target computer and a serial device under control of the host computer.

The invention will be more clearly understood from the following description of some preferred embodiments thereof,

given by way of example only with reference to the accompanying drawings in which:-

Fig. 1 is a block diagram showing a capture device of the invention, in use;

Fig. 2 is a detailed drawing showing a screen capture circuit of the device; and

Figs. 3, 4 and 5 are block diagrams showing different configurations for use of the capture device.

Referring to the drawings, and initially to Fig. 1 there is illustrated a capture device of the invention, indicated generally by the reference numeral 1. The device 1 includes a serial capture circuit 3 and a host computer bus interface 4. The bus interface 4 is connected to a host computer 5 by a cable interface 6. A screen capture circuit 2 is connected in a target computer 7 and to an interface circuit 8. The serial capture circuit 3 includes a microprocessor and a memory storing simulation programs. It is connected to transmit and receive lines 9 and 10 respectively connecting the target computer 7 with a serial device 11. The serial device may be a computer, a terminal, a tablet, a mouse or any other serial device.

Referring now to Fig. 2, the screen capture circuit 2 is illustrated in more detail together with portion of the target computer 7. Portions of the target computer 7 which are illustrated are a screen memory 15, which is connected to a graphics display circuit 16, which is in turn connected to a target screen 17. These circuits are conventional and require no further description. The screen capture circuit 2 comprises a decode circuit 18 which is connected to the output of the graphics display circuit 16. The decode circuit 18 is constructed to monitor the position and clock signals of pixel control signals and to generate hexadecimal bytes representing displayed pixels. The position and clock signals are used to generate these bytes and to generate control signals for the memory pointer circuit 20. The decode circuit 18 is connected to a capture memory 19 and a memory pointer circuit 20. The capture memory 19 is connected to an arbitration circuit 21 which is in turn connected to the bus interface 4.

In operation, as the target computer 7 operates, screen data is transmitted to the screen memory 15 from where it is read by the graphics display circuit 16, which in turn generates control signals for display of pixels at the target screen 17. The pixel control signals include various electronic signals such as pixel data lines, horizontal and vertical synchronous signals, clock signals and blank signals. The pixel control signals are delivered directly to the decode circuit 18, in parallel with delivery to the target screen 17. The decode

circuit 18 generates hexadecimal memory bytes from the pixel control signals, which memory bytes are transmitted to the capture memory 19 for storage. Monitored position signals within the pixel control signals are used to address these bytes and to generate control signals for the memory pointer circuit 20 to allow the host computer to read the capture memory 19 in an intelligent manner via the bus interface 4 and the arbitration circuit 21 (which controls access of the bus interface 4 to the capture memory 19). The position signals within the pixel control signals which are used for generation of the control signals for the memory pointer circuit 20 are horizontal and vertical synchronous signals and clock signals.

In addition, the decode circuit 18 is constructed to allow examination of individual pixels, which is useful where a computer test engineer wishes to filter out certain colour pixels for storage and/or comparison.

It will thus be appreciated that the screen capture circuit allows a user to examine the actual signals controlling the target screen so that such things as different fonts or even individual pixels may be monitored. The user is thus given a picture of what exactly is displayed rather than a representation of what should be displayed on the target screen.

Simultaneously with monitoring of what is displayed on the target screen, the capture device 1 allows capture of serial data on serial lines such as the lines 9 and 10 connecting the target computer 7 to the serial device 11. The serial data is also delivered to the host computer 5 in a suitable format by the serial capture circuit 3 for storage and/or verification. As shown by the interrupted lines of Fig. 1, the serial capture circuit 3 may simply monitor the transmitted and received serial data.

Referring now to Figs. 3, 4 and 5 other arrangements are illustrated which show the manner in which the serial capture circuit 3 may be used. In Fig. 3, an arrangement is shown whereby the serial capture circuit generates signals which simulate received signals for the target computer 7 and monitors the subsequent transmit signals for line 9. This is carried out under control of the host computer 5. The reverse situation is illustrated in Fig. 4 in which the serial capture circuit 3 generates simulated transmit signals which are delivered by the serial capture circuit 3 to the serial device 11. The signals are monitored by the host computer 5. Another arrangement is illustrated in Fig. 5 whereby the serial capture circuit 3 simulates both receive and transmit signals for the target computer 7 and the serial device 11, respectively.

It will thus be appreciated that the invention provides a capture device which is versatile in operation as it allows capture of both screen and serial signals of a target computer.

The invention is not limited to the embodiments hereinbefore described, but may be varied in construction and detail.

CLAIMS

1. A computer testing capture device comprising a screen capture circuit comprising:-

a decode circuit for decoding pixel control signals of a target screen and generating decoded data bytes representing displayed pixels;

a capture memory for the decoded data bytes;

an output interface for reading the decoded data for transmission to a host computer; and a capture memory address pointer circuit for directing access of the output interface to the capture memory, and wherein the decode circuit comprises means for controlling the pointer circuit in response to position control signals within the pixel control signals.

2. A device as claimed in claim 1, further comprising a serial capture circuit comprising means for monitoring and simulation of serial data flow between a target computer and a serial device under control of the host computer.

3. A device substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number
9125588.5

Relevant Technical fields

(i) UK Cl (Edition K) B3V

(ii) Int Cl (Edition 5) B23K

Search Examiner
D N P BUTTERS

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search
7 FEBRUARY 1992

Documents considered relevant following a search in respect of claims ALL

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	GB 1229876 (LASER TECHNIQUE) (SEE FIGURE 3)	CL 2

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

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&: Member of the same patent family, corresponding document.

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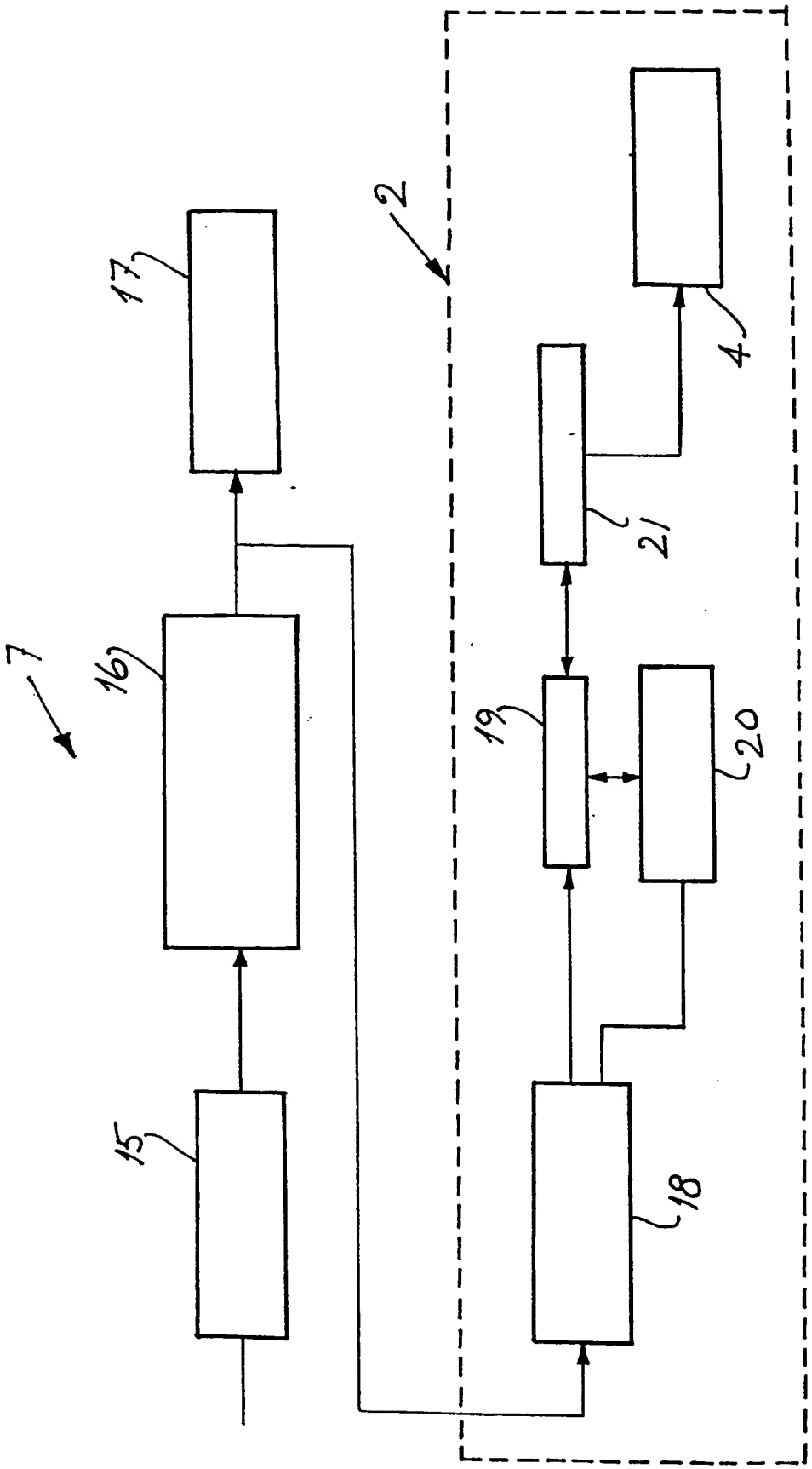

Fig. 2

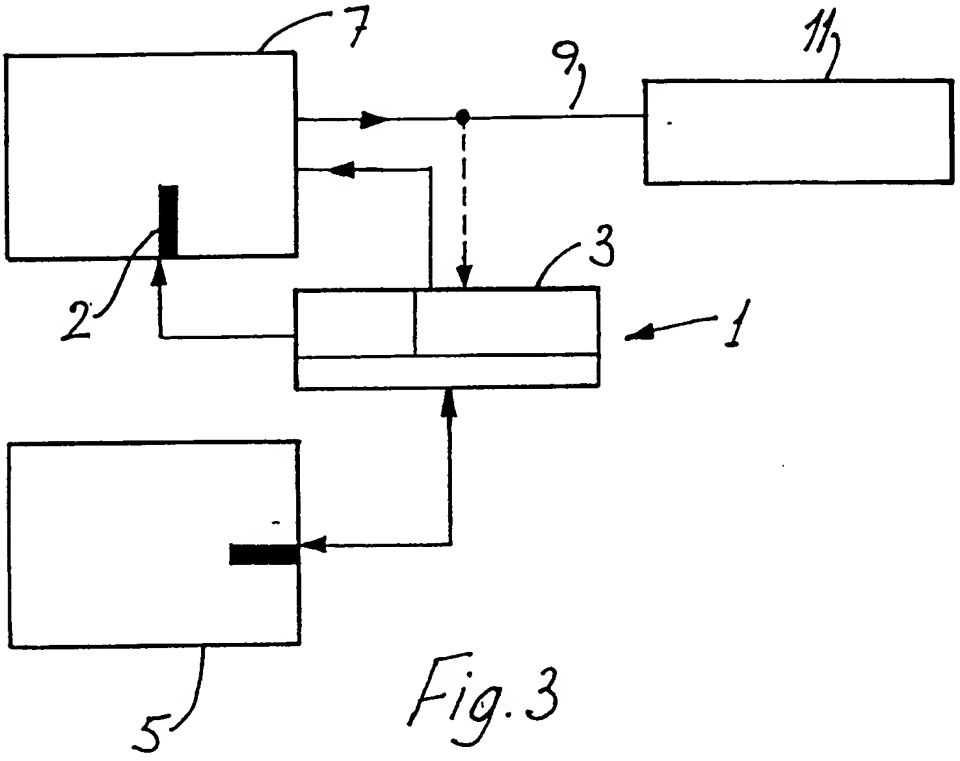

Fig.3

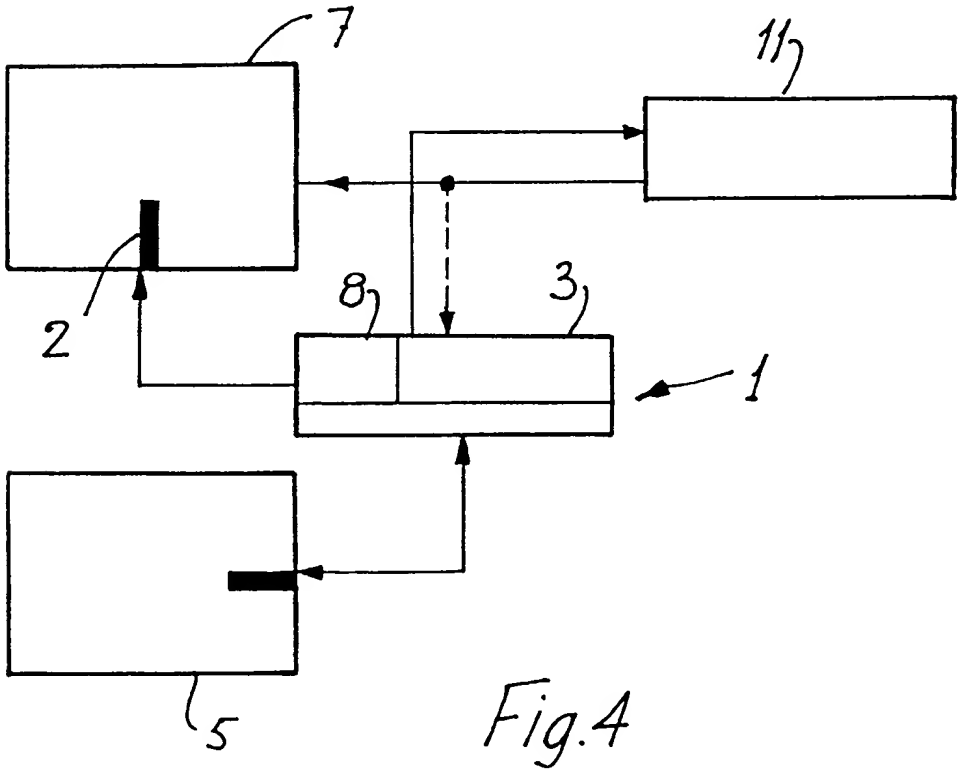

Fig.4

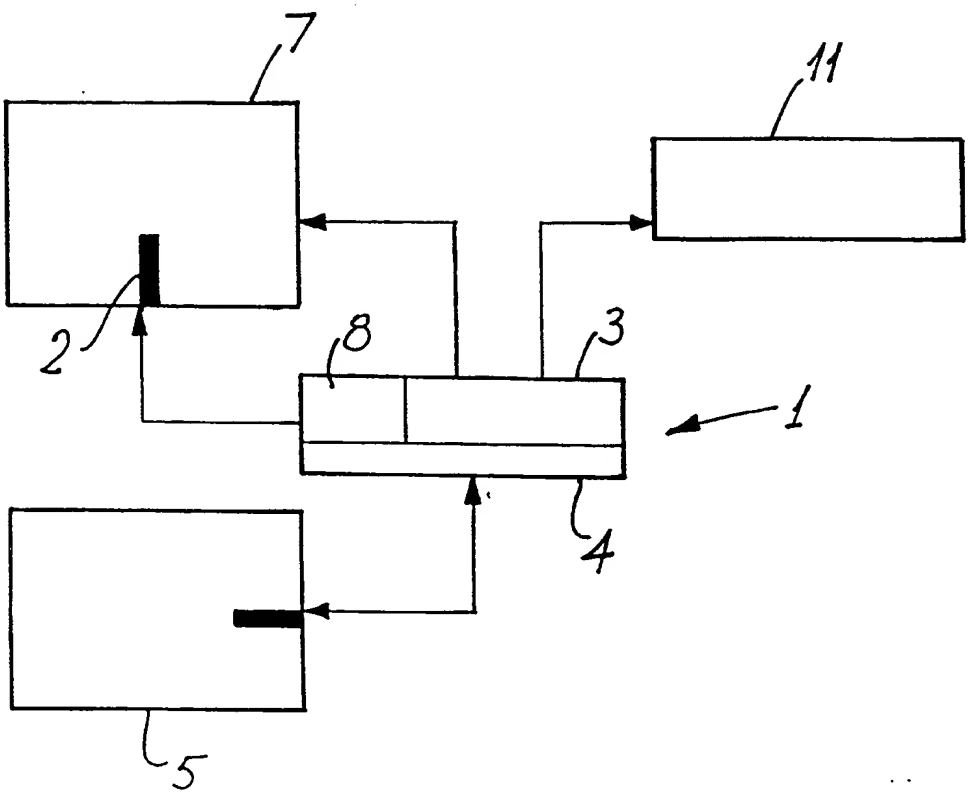

Fig.5